GATE DRIVE CIRCUIT

CROSS-REFERENCE TO RELATED APPLICATION

This application is based upon and claims the benefit of priority from Japanese Patent Application No. 2015-051407, filed March 13, 2015; the entire contents of which are incorporated herein by reference.

FIELD

Embodiments described herein relate generally to a gate drive circuit.

BACKGROUND

A high voltage which is equal to or higher than 10 V is needed to be applied to a gate of a power semiconductor element which switches a high current, such as an IGBT. Thus, the gate of the power semiconductor element is usually driven by a high-side MOS transistor to which a high voltage is applied and a low-side MOS transistor. The high-side MOS transistor and the low-side MOS transistor are coupled in series between a power supply voltage node and a ground node. For this reason, if both the transistors are turned on at the same timing, a through current flows between the power supply voltage node and the ground node, and thereby power loss occurs. Thus, a control in which the high-side MOS transistor and the low-side MOS transistor are not turned on at the same time is necessary.

In addition, a control in which a through current also does not flow through an inside of a gate drive circuit which controls the high-side MOS transistor and the low-side MOS transistor is necessary.

An example of related art includes JP-A-2011-101217.

DESCRIPTION OF THE DRAWINGS

FIG. 1 is a block diagram of a gate drive circuit according to a first embodiment.

FIG. 2 is a circuit diagram illustrating an example of an internal configuration of first to third timing control units.

FIG. 3 is a signal waveform diagram of the gate drive circuit according to the first embodiment.

FIG. 4 is a circuit diagram illustrating an internal configuration of first to third timing control units according to a second embodiment.

FIG. 5 is a signal waveform diagram of the gate drive circuit according to the second embodiment.

FIG. 6 is a circuit diagram illustrating an internal configuration of a first timing control unit according to a third embodiment.

FIG. 7 is a block diagram of a gate control circuit according to a fourth embodiment.

FIG. 8 is a circuit diagram illustrating an internal configuration of an overcurrent detection circuit.

FIG. 9 is a circuit diagram illustrating an example of internal configurations of a soft turn-off circuit and a mirror clamp circuit.

FIG. 10 is a circuit diagram illustrating an example of internal configurations of a restart circuit and first to third timing control units.

FIG. 11 is a circuit diagram illustrating an example of internal configuration of the third timing control unit.

FIG. 12 is a signal waveform diagram of a gate drive circuit according to a fourth embodiment.

DETAILED DESCRIPTION

[0005]

Exemplary embodiments provide a gate drive circuit which controls in such a manner that a through current does not flow.

[0006]

According to one embodiment, there is provided a gate drive circuit includes a first PMOS transistor that is coupled between a first reference voltage node and a first output node; a first NMOS transistor that is coupled between the first output node and a second reference voltage node whose voltage level is lower than that of the first reference voltage node; a second PMOS transistor that is coupled between the first reference voltage node and a second output node; a second NMOS transistor that is coupled between the second output node and the second reference voltage node; and a gate control circuit that generates each gate signal of the first PMOS transistor, the first NMOS transistor, the second PMOS transistor, and the second NMOS transistor, based on an input signal, in which the gate control circuit includes a first timing control unit that, before a potential of the first output node is decreased from a high potential to a low potential, decreases a potential of the second output node from a high potential to a low potential, and before a potential of the second output node is increased from a low potential to a high potential, increases a potential of the first output node from a low potential to a high potential; a second timing control unit that, before one of the first PMOS transistor and the first NMOS transistor is changed from OFF to ON, changes the other of those from ON to OFF, and before the other is changed from OFF to ON, changes the one from ON to OFF; and a third timing control unit that, before one of the second PMOS transistor and the second NMOS transistor is changed from OFF to ON, changes the other of those from ON to OFF, and after the one is changed from ON to OFF, changes the other from OFF to ON.

[0008]

Hereinafter, exemplary embodiments will be described with reference to the drawings. In the following embodiments, a characteristic configuration and an operation of a gate drive circuit will be mainly described, but a configuration and an operation which are omitted in the following description may exist. However, the configuration and the operation which are omitted are also included in a range of the present embodiments.

First Embodiment

[0009]

FIG. 1 is a block diagram of a gate drive circuit 1 according to a first embodiment. The gate drive circuit 1 of FIG. 1 includes a first PMOS transistor Q2 and a first NMOS transistor Q3 which drive a high-side PMOS transistor (third transistor) Q1, a second PMOS transistor Q5 and a second NMOS transistor Q6 which drive a low-side NMOS transistor (fourth transistor) Q4, and a gate control circuit 2 which generates each gate signal of the transistors Q2, Q3, Q5 and Q6.

[0010]

The high-side PMOS transistor Q1 and the low-side NMOS transistor Q4 are normally attached to an outside of an IC of the gate drive circuit. However, the high-side PMOS transistor Q1 and the low-side NMOS transistor Q4 may be embedded in the IC of the gate drive circuit 1.

[0011]

The high-side PMOS transistor Q1 and the low-side NMOS transistor Q4 are used for driving a power semiconductor element (fifth transistor) Q7 such as an IGBT. The power semiconductor element Q7 is also attached to an outside of an IC of the gate drive circuit 1.

[0012]

The high-side PMOS transistor Q1 is coupled between a power supply voltage VCCH node and a gate of the power semiconductor element Q7. In addition, the low-side NMOS transistor Q4 is coupled between a ground node and the gate of the power semiconductor element Q7. In FIG. 1, a resistor element R1 is coupled between a drain of the high-side PMOS transistor Q1 and the gate of the power semiconductor element Q7, and in the same manner, a resistor element R2 is coupled between a drain of the low-side NMOS transistor Q4 the gate of the power semiconductor element Q7, but the resistor elements R1 and R2 may be omitted.

[0013]

The high-side PMOS transistor Q1 and the low-side NMOS transistor Q4 are, for example, laterally diffused metal oxide semiconductor (LDMOS) transistors. Gate breakdown voltages of the transistors are, for example, equal to or less than 6 V, and drain-source breakdown voltages are, for example, 40 V.

[0014]

The first PMOS transistor Q2 is coupled between the power supply voltage VCCH node and a gate of the high-side PMOS transistor Q1. The first NMOS transistor Q3 is coupled between the gate of the high-side PMOS transistor Q1 and a ground node.

[0015]

In the same manner, the second PMOS transistor Q5 is coupled between the power supply voltage VCCH node and a gate of the low-side NMOS transistor Q4. The second NMOS transistor Q6 is coupled between the gate of the low-side NMOS transistor Q4 and a ground node.

[0016]

In FIG. 1, resistor element R3 and R4 are coupled between each drain of the first PMOS transistor Q2 and the first NMOS transistor Q3, and a gate of the high-side PMOS transistor Q1, and resistor element R5 and R6 are coupled between each drain of the second PMOS transistor Q5 and the second NMOS transistor Q6, and a gate of the low-side NMOS transistor Q4, but the resistor elements R3 to R6 may be omitted.

[0017]

The gate control circuit 2 generates signals for controlling the respective gate voltages of the first PMOS transistor Q2, the first NMOS transistor Q3, the second PMOS transistor Q5, and the second NMOS transistor Q6, in synchronization with an input signal PWM of the gate drive circuit 1. The input signal PWM is a pulse width modulation (PWM) signal which is pulse-width-modulated. By turn-on or turn-off of the transistors, the high-side PMOS transistor Q1 and the low-side NMOS transistor Q4 are also turned on or off, and thereby a voltage signal VIGBT\_GATE which is synchronized with the input signal PWM is output from the respective drains of the high-side PMOS transistor Q1 and the low-side NMOS transistor Q2, and is input to the gate IGBT\_GATE of the power semiconductor element Q7.

[0018]

As illustrated in FIG. 1, the gate control circuit 2 includes a first timing control unit 3, a second timing control unit 4, and a third timing control unit 5.

[0019]

The first timing control unit 3 performs a timing control in which, before a gate of the high-side PMOS transistor Q1 is decreased to a low potential from a high potential, a gate of the low-side NMOS transistor Q4 is decreased to a low potential from a high potential, and before a gate of the low-side NMOS transistor Q4 is increased to a high potential from a low potential, a gate of the high-side PMOS transistor Q1 is increased to a high potential from a low potential.

[0020]

The second timing control unit 4 performs a timing control in which, before one of the first PMOS transistor Q2 and the first NMOS transistor Q3 is changed to ON from OFF, the other of those is changed to OFF from ON, and before the other is changed to ON from OFF, the one is changed to OFF from ON.

[0021]

The third timing control unit 5 performs a timing control in which, before one of the second PMOS transistor Q5 and the second NMOS transistor Q6 is changed to ON from OFF, the other of those is changed to OFF from ON, and after the one is changed to OFF from ON, the other is changed to ON from OFF.

[0022]

FIG. 2 is a circuit diagram illustrating an example of internal configurations of the first to third timing control units 3 to 5. The first timing control unit 3 includes inverters IV1 to IV4, and a first delay circuit 6. The inverters IV1 and IV2 are coupled in cascade. The inverter IV1 inverts the input signal PWM, and the inverter IV2 outputs a signal having the same logic as that of the input signal PWM. An output signal of the inverter IV2 is input to the third timing control unit 5. The inverter IV3 outputs an inverted signal of the output signal of the invert IV1, and inputs the inverted signal to the first delay circuit 6.

[0023]

The first delay circuit 6 delays the output signal of the inverter IV3 by a first time td\_master, and outputs the delayed signal. Time length of the first time td\_master may be able to be arbitrarily adjusted, and may be delayed by a predetermined fixed time. The inverter IV4 inverts an output signal of the first delay circuit 6 and outputs the inverted signal.

[0024]

As will be described later, ON timing of the high-side PMOS transistor Q1 and the low-side NMOS transistor Q4 is shifted by the first time td\_master which is delayed by the first delay circuit 6. By doing this, a through current does not flow from the power supply voltage VCCH node to the ground node via the high-side PMOS transistor Q1 and the low-side NMOS transistor Q4. The second timing control unit 4 and the third timing control unit 5 shifts timing in which a gate voltage of the high-side PMOS transistor Q1 and a gate voltage of the low-side NMOS transistor Q4 are changed, using the first time td\_master.

[0025]

The second timing control unit 4 includes a second delay circuit 7, a third delay circuit 8, a first NMOS gate control circuit 9, and a first PMOS gate control circuit 10.

[0026]

The second delay circuit 7 performs a timing control of raising a gate signal of the first NMOS transistor Q3, after being delayed by a second time td1 from rising timing of a gate signal of the first PMOS transistor Q2.

[0027]

The second delay circuit 7 delays falling timing of an input signal to the second delay circuit 7 by a second time td1, inverts the delayed signal, and outputs the inverted signal. Rising timing of the input signal to the second delay circuit 7 is inverted and is output without being changed.

[0028]

The third delay circuit 8, and a NAND gate G1 and an inverter IV5 which are on a rear side of the third delay circuit delay a third time td2 from falling timing of the gate signal of the first NMOS transistor Q3, and thereafter performs a timing control in which the gate signal of the first PMOS transistor Q2 falls.

[0029]

The third delay circuit 8 also delays the falling timing of the input signal to the third delay circuit by the third time, inverts the delayed signal, and outputs the inverted signal. Rising timing of the input signal of the third delay circuit 8 is inverted and is output without being changed.

[0030]

The first NMOS gate control circuit 9 includes a NAND gate G2, inverters IV6 and IV7, and an OR gate G3. The first NMOS gate control circuit 9 controls a gate voltage of the first NMOS transistor Q3. An output signal of the inverter IV7 in the first NMOS gate control circuit 9 becomes a gate voltage of the first NMOS transistor Q3.

[0031]

The second PMOS gate control circuit 2 includes a level-up circuit 11, a level-down circuit 12, a NOR circuit G4, and an inverter IV8. The first PMOS gate control circuit 10 controls a gate voltage of the first PMOS transistor Q2. An output signal of the inverter IV8 in the first PMOS gate control circuit 10 becomes a gate voltage of the first PMOS transistor Q2.

[0032]

The third timing control unit 5 includes a fourth delay circuit 13, a second NMOS gate control circuit 14, a fifth delay circuit 15, and a second PMOS gate control circuit 16.

[0033]

The fourth delay circuit 13 delays a signal having the same logic as that of the input signal PWM, specifically, an output signal of the inverter IV2 by a fourth time DT1.

[0034]

The second NMOS gate control circuit 14 includes a NAND gate G5 and an inverter IV9. The NAND gate G5 outputs a signal which is obtained by performing a logical product of input and output signals of the fourth delay circuit 13 and by inverting the signal. The inverter IV9 inverts an output signal of the NAND gate, outputs the inverted signal, and supplies a gate of the second NMOS transistor Q6 with the output signal.

[0035]

The fifth delay circuit 15 delays an output signal of the level-up circuit 11 by a fifth time DT2. The second PMOS gate control circuit 16 includes an AND gate G6, and an inverter IV10. The AND gate G6 outputs a signal which is obtained by performing a logical product of input and output signals of the fifth delay circuit 15. The inverter IV10 inverts an output signal of the AND gate G6, outputs the inverted signal, and supplies a gate of the second PMOS transistor Q5 with the output signal.

[0036]

FIG. 3 is a signal waveform diagram of the gate drive circuit 1 according to the first embodiment. In the signal waveform diagrams of FIG. 3 or later, potentials of each signal path are described as “low” or “high”, and signal amplitudes in a horizontal axis direction which represents a potential are represented so as to be the same, but actually, voltage amplitudes of each signal are respectively different from each other.

[0037]

To begin with, if a voltage VPWM of the input signal PWM becomes high from low in time t1, an output of the first delay circuit 6 illustrated in FIG. 2 becomes low from high after the first time td\_master from the time t1. As a result, an output of the NAND gate G1 becomes high, an output of the inverter IV5 in a subsequent stage of the NAND gate becomes low, and an output VGP1 of the inverter IV8 which is an output of the first PMOS gate control circuit 10 becomes high from low (time t2).

[0038]

In addition, if the output of the inverter IV5 becomes low, an input of the fifth delay circuit 15 becomes low. Thus, an output of the AND gate G6 becomes low, and an output VGP2 of the inverter IV10 becomes high (time t2).

[0039]

In addition, if the input signal PWM becomes high from low, an output of the inverter IV2 in the first timing control unit 3 becomes high, an output of the fourth delay circuit 13 becomes high after being delayed by fourth time DT1 from the time t1. As a result, the NAND gate G5 in a subsequent stage of the fourth delay circuit 13 becomes low, and a gate of the second NMOS transistor Q6 becomes high. Thus, the second NMOS transistor Q6 is turned on (time t3).

[0040]

Meanwhile, if all of the gate potentials VGP1 and VGP2 of the first PMOS transistor Q2 and the second PMOS transistor Q5 become high, the NOR gate G4 becomes low, and the input of the second delay circuit 7 also becomes low. An output of the second delay circuit 7 becomes high after being delayed by the second time td1 from time in which an input of the second delay circuit 7 is changed from high to low. As a result, an output of the NAND gate G2 becomes low, an output VGN1 of the inverter IV7 in a subsequent stage of the NAND gate G2 becomes high, and the fist NMOS transistor Q3 is turned on (time t4).

[0041]

To sum up the above, the gate potentials VGP1 and VGP2 of the first PMOS transistor Q2 and the second PMOS transistor Q5 become high after being delayed by approximately the first time td\_master from the time t1. In addition, a gate potential VGN2 of the second NMOS transistor Q6 becomes high after being delayed by fourth time DT1 from the time t1. The fourth time DT1 is longer than the first time td\_master, and thus the second NMOS transistor Q6 is turned on after the first PMOS transistor Q2 and the second PMOS transistor Q5 are turned off. Furthermore, the first NMOS transistor Q3 is turned on after being delayed by the second time td1 from time in which the first PMOS transistor Q2 is turned off.

[0042]

Thereafter, if the input signal PWM is changed from high to low in the time t2 (time t5), an output of the inverter IV2 in the first timing control unit 3 is changed from high to low. Thus, the NAND gate G5 becomes high, and an output potential VGN2 of the inverter IV9 in a subsequent stage of the NAND gate G5 becomes low. As a result, the second NMOS transistor Q6 is turned off (time t5).

[0043]

In addition, after the first time td\_master passes from the time t2, an output of the first delay circuit 6 becomes high. Thus, an output of the inverter IV6 becomes low, an output of the NAND gate G2 in a subsequent state of the inverter IV6 becomes high, and the output potential VGN1 of the inverter IV7 in a subsequent stage of the NAND gate G2 becomes low. As a result, the first NMOS transistor Q is turned off (time t6).

[0044]

In addition, if the output potential VGN1 of the inverter IV7 becomes low, an input of the third delay circuit 8 which is an output of the OR gate G3 becomes low. The third delay circuit 8 becomes high after being delayed by the third time td2 from time in which an input of the third delay circuit 8 is in a low level. Thus, an output of the NAND gate G1 in a subsequent stage of the third delay circuit 8 becomes low, an output of the inverter IV5 in a subsequent stage of the NAND gate G1 becomes high, an output of the level-up circuit 11 in a subsequent stag of the invert IV5 becomes high, and an output potential VGP1 of the inverter IV8 in the subsequent stage of the level-up circuit 11 becomes low. As a result, the first PMOS transistor Q2 is turned on (time t7).

[0045]

In addition, if an output of the level-up circuit 11 becomes high, an input of the fifth delay circuit 15 also becomes high. An output of the fifth delay circuit 15 becomes high after being delayed by the fifth time DT2 from time in which an input of the fifth delay circuit 15 is in a high level, the AND gate G6 in a subsequent stage of the fifth delay circuit 15 also becomes high, and the inverter IV10 in a subsequent stage of the AND gate G6 also becomes low. As a result, the second PMOS transistor Q5 is turned on (time t8).

[0046]

To sum up the above, if the input signal PWM becomes low from high in time t5, the second NMOS transistor Q6 is immediately turned off, and the first NMOS transistor Q3 is turned off after being delayed by the first time td\_master from the time t5. Subsequently, the first NMOS transistor Q3 is turned off, and thereby the first PMOS transistor Q2 is turned off after being delayed by the third time td2, and the second PMOS transistor Q5 is turned off after being delayed by the fifth time DT2 from time in which the first PMOS transistor Q2 is turned off.

[0047]

In this way, in the first embodiment, when the input signal PWM becomes high from low, gate voltages of the transistors Q2, Q3, Q5, and Q6 are shifted and changed by the first delay circuit 6, the second delay circuit 7, and the fourth delay circuit 13. When the input signal PWM becomes low from high, the gate voltages of the transistors Q2, Q3, Q5, and Q6 are shifted and changed by the first delay circuit 6, the third delay circuit 8, and the fifth delay circuit 15. As a result, a current which passes through the high-side PMOS transistor Q1 and the low-side NMOS transistor Q4, a current which passes through the first PMOS transistor Q2 and the first NMOS transistor Q3, and a current which passes through the second PMOS transistor Q5 and the second NMOS transistor Q6 and which does not turn on the second PMOS transistor Q5 and the second NMOS transistor Q6 at the same time, are not generated.

[0048]

In addition, the gate drive circuit 1 according to the present embodiment drives the high-side PMOS transistor Q1 and the low-side NMOS transistor Q4 which have low gate breakdown voltages and are low cost, and thereby a gate IGBT\_GATE of the power semiconductor element Q7 which is driven by the transistors Q1 and Q4 can be fully swung. As a result, s drive efficiency of the power semiconductor element Q7 is increased.

Second Embodiment

[0049]

In a second embodiment, a circuit configuration of the gate control circuit 2 is simpler than that of the first embodiment.

[0050]

The gate control circuit 2 according to the second embodiment includes the first timing control unit 3, the second timing control unit 4, and a third timing control unit 5, in the same manner as FIG. 2. Among these, circuit configurations of the first timing control unit 3 and the third timing control unit 5 are significantly different from those according to the first embodiment.

[0051]

FIG. 4 is a circuit diagram illustrating internal configurations of the first to third timing control units 3 to 5 according to the second embodiment. The first timing control unit 3 of FIG. 4 includes the first delay circuit 6, an AND gate G11, and an inverter V11.

[0052]

The first delay circuit 6 delays the input signal PWM by the first time DT. The AND gate G11 outputs a logical product signal of the input signal and the output signal of the first delay circuit 6. The inverter IV11 inverts an output of the AND gate G11 and outputs the inverted signal.

[0053]

The second timing control unit 4 of FIG. 4 is configured by approximately the same circuit as the second timing control unit 4 of FIG. 1. In addition, the third timing control unit 5 of FIG. 4 is configured by approximately the same circuit as the second timing control unit 4. More specifically, the third timing control circuit 5 includes a fourth delay circuit 21 corresponding to the second delay circuit 7 in the second timing control unit 4, a fifth delay circuit 22 corresponding to the third delay circuit 8, a second NMOS gate control circuit 14, and a second PMOS gate control circuit 16. The second NMOS gate control circuit 14 includes NAND gates G13 and G14, and inverters IV14, IV17, and IV18. A second PMOS gate control circuit 16 includes a level-up circuit 23, a level-down circuit 24, and inverters IV15 and IV16. If an input becomes low from high, the second and fourth delay circuits 7 and 21 in the second and third timing control units 4 and 5 delay the input by the same time (second and fourth times) td1 and makes high. In addition, if an input becomes low from high, the third and fifth delay circuits 8 and 22 are delayed by the same time (third and fifth times) td2 and becomes high.

[0054]

FIG. 5 is a signal waveform diagram of the gate drive circuit 1 according to the second embodiment. To begin with, if the input signal PWM becomes high from low in time t1, an output of the OR gate G12 in the third timing control unit 5 becomes low, and an output of the inverter IV13 on the subsequent side thereof becomes low. Thus, an output of the NAND gate G13 on the subsequent side becomes high, an output of the inverter IV14 on the subsequent side becomes low, and subsequently, an output of the level-up circuit 23 becomes low, an output potential VGP2 of the inverter IV15 becomes high, and the second PMOS transistor Q5 is turned off.

[0055]

If an output of the inverter IV15 becomes high, an output of the inverter IV16 becomes low, an input of the fourth delay circuit 21 which is an output of the level-down circuit 24 becomes low. The input becomes low, and then an output of the fourth delay circuit 21 becomes high after being delayed by the fourth time td1. Thus, an output of the NAND gate G14 becomes low, and an output potential VGN2 of the inverter IV17 on the subsequent side thereof becomes high. As a result, the second NMOS transistor Q6 is turned on (time t2).

[0056]

An output of the first delay circuit 6 becomes high after being delayed by the first time DT from the time in which the input signal PWM is changed from low to high, and in the same manner, the AND gate G11 also becomes high after being delayed by the first time, as the input signal PWM is changed from low to high, and an output of the inverter IV11 on the subsequent side becomes low. Thus, in the same manner as the second timing control unit 4 of FIG. 2, a gate potential VGP1 of the first PMOS transistor Q2 becomes high, and thereby the first PMOS transistor Q2 is turned off (time t3). Thereafter, in the same manner as the second timing control unit 4 of FIG. 3, the first PMOS transistor Q2 is turned off, and then the second PMOS transistor Q5 is turned off (time t4) after being delayed by the second time td1.

[0057]

Thereafter, if the input signal PWM becomes low from high in time t5, an output of the AND gate G11 becomes low, an output of the inverter IV11 on the subsequent side thereof becomes high. Thus, an output of the inverter IV6 becomes low, an output of the NAND gate G2 on the subsequent side thereof becomes high, and an output potential VGN1 of the inverter IV7 on the subsequent side thereof becomes low. Thus, the first NMOS transistor Q3 is turned off (time t5).

[0058]

If the output of the inverter IV7 becomes low, an output of the third delay circuit 8 becomes high after being delayed by the third time td2. Thus, in the same manner as the second timing control unit 4 of FIG. 2, a gate potential VGP1 of the first PMOS transistor Q2 becomes low, and thereby the first PMOS transistor Q2 is turned on (time t6).

[0059]

In addition, if the input signal PWM becomes low from high in time t2, an output of the first delay circuit 6 becomes low after being delayed by the first time DT. Thus, an output of the OR gate G12 becomes low, an output of the inverter IV 13 on the subsequent side thereof becomes high, and an output of the inverter IV18 on the subsequent side thereof becomes low. Thus, an output of the NAND gate G14 becomes high, and an output potential VGN2 of the inverter IV17 on the subsequent side thereof becomes low. Thus, the second NMOS transistor Q6 is turned off (time t7).

[0060]

If an output potential VGN2 of the inverter IV17 becomes low, an output of the fifth delay circuit 22 becomes high after being delayed by the fifth time td2. Thus, an output of the NAND gate G13 becomes low, an output of the inverter IV14 on the subsequent side thereof becomes high, an output of the level-up circuit 23 on the subsequent side thereof becomes high, and an output potential VGP2 of the inverter IV15 on the subsequent side thereof becomes low. As a result, the second PMOS transistor Q5 is turned on (time t8).

[0061]

In this way, in the second embodiment, the gate voltages are controlled by the first delay circuit 6, in such a manner that the high-side PMOS transistor Q1 and the low-side NMOS transistor Q4 are not simultaneously turned on. In addition, the gate voltages are controlled by the second to fifth delay circuits 7, 8, 21, and 22, in such a manner that the first PMOS transistor Q2 and the first NMOS transistor Q3 are not simultaneously turned on. In the same manner, the gate voltages are controlled in such a manner that the second PMOS transistor Q5 and the second NMOS transistor Q6 are not simultaneously turned on.

[0062]

The second embodiment is configured by a simpler circuit than that of the first embodiment, and thus, it is possible to decrease a through current, in the same manner as the first embodiment.

Third Embodiment

[0063]

In a third embodiment, only an internal configuration of a first timing control unit 3 is different from that of the second embodiment.

[0064]

FIG. 6 is a circuit diagram illustrating an internal configuration of the first timing control unit 3 according to the third embodiment. The first timing control unit 3 of FIG. 6 includes a logic determination unit 25 in addition to the circuit configuration of FIG. 4. Based on a logic selection signal SEL, the logic determination unit 25 determines whether to set the signal logics of an input signal PWM and a gate signal VIGBT\_GATE of a power semiconductor element Q7 which is driven by a gate drive circuit 1 to be identical or to be reversed to each other. For example, if the logic selection signal SEL is high, signal logics of the input signal PWM and the gate signal VIGBT\_GATE of the power semiconductor element Q7 are performed in the same manner, and if the logic selection signal SEL is low, signal logics of the input signal PWM and the gate signal VIGBT\_GATE of the power semiconductor element Q7 are performed in reverse.

[0065]

If the logic selection signal SEL is low, for example, a high-side transistor Q1 illustrated in FIG. 7 is configured by an N type transistor and a low-side transistor Q4 which are illustrated in FIG. 7 is configured by an P type transistor, and according to this, output logics of a soft turn-off circuit 32 and a mirror clamp circuit 33 are also required to be reversed. As a result, according to the third embodiment, simply by switching the logic of the logic selection signal SEL, a power semiconductor element Q7 can be driven by the logic in which the input signal PWM is inverted.

[0066]

The logic determination unit 25 may be added to the first timing control unit 3 illustrated in FIG. 2, and in addition, may be added to a first timing control unit 3 according to a fourth embodiment which will be described later.

Fourth Embodiment

[0067]

A fourth embodiment includes an overcurrent detection function, a soft turn-off function, a mirror clamp function, and a restart function which are added to the gate control circuit 2 according to the second embodiment.

[0068]

FIG. 7 is a block diagram of a gate control circuit 2 according to a fourth embodiment. The gate control circuit 2 of FIG. 7 includes an overcurrent detection circuit 31, a soft turn-off circuit 32, a mirror clamp circuit 33, and a restart circuit 34, in addition to the first timing control unit 3, a second timing control unit 4, and a third timing control unit 5.

[0069]

FIG. 8 is a circuit diagram illustrating an internal configuration of the overcurrent detection circuit 31. The overcurrent detection circuit 31 of FIG. 8 includes a first comparator 35, an eighth delay circuit 36, a NAND gate G21, inverters IV21 and IV22, OR gates G22 and G23, a second comparator 37, an AND gate G24, an S/R flip-flop 38.

[0070]

An overcurrent detection signal VSEN is input to the first comparator 35. The overcurrent detection signal is, for example, an emitter voltage of the power semiconductor element Q7. If an emitter current of the power semiconductor element Q7 is in an overcurrent state, an emitter voltage is increased. Thus, by feeding back the emitter voltage to the overcurrent detection circuit 31 as an overcurrent detection signal, it is possible to detect whether to be an overcurrent state or not.

[0071]

The first comparator 35 outputs 5 V, if a voltage level of the overcurrent detection signal is higher than, for example, 0.75 V, and outputs 0 V, if the voltage level of the overcurrent detection signal is equal to or lower than 0.75 V. The eighth delay circuit 36 delays an output signal of the first comparator 35 by an eighth delay time (for example, 1 ms) and outputs the delayed signal.

[0072]

The NAND gate G21 outputs a logical product inversion signal of an output signal of the first comparator 35 and an output signal of the eighth delay circuit 36, the inverter IV21 outputs an inverted signal of an output of the NAND gate G21, and the signal is input to a set terminal of the S/R flip-flop 38 via the OR gate G22. In addition, the OR gate G23 outputs a logical sum signal of a power-on-reset signal POR and an output signal of an inverter IV42 in a restart circuit 34 which will be described later, and the signal is input to a reset terminal of the S/R flip-flop 38.

[0073]

The second comparator 37 outputs 5 V if a gate voltage VIGBT\_GATE of the power semiconductor element Q7 is lower than 3. 5 V, and outputs 0 V if the gate voltage VIGBT\_GATE of the power semiconductor element Q7 is equal to or higher than 3. 5 V. A voltage value of 3.5 V which is compared by the second comparator 37 is an example, and may be an arbitrary voltage in a range between 2 V and 3.5 V.

[0074]

The AND gate G24 outputs a logical product signal of a Q output signal of the S/R flip-flop 38 and an output signal of the second comparator 37 as an overcurrent error signal 2dan\_err\_H, and the inverter IV22 outputs an inverted signal 2dan\_err\_L thereof.

[0075]

In this way, the overcurrent detection circuit 31 of FIG. 8 detects the emitter voltage of the power semiconductor element Q7, and determines whether to be in an overcurrent state or not. When being in an overcurrent state, the overcurrent detection circuit 31 outputs an overcurrent signal VSC\_H as a high potential. In addition, thereafter, the overcurrent detection circuit 31 outputs the signal 2dan\_err\_H as a high potential if the gate voltage of the power semiconductor element Q7 is equal to or higher than 3.5 V, and outputs the signal 2dan\_err\_H as a low potential if the gate voltage is lower than 3.5 V.

[0076]

FIG. 9 is a circuit diagram illustrating an example of internal configurations of the soft turn-off circuit 32 and the mirror clamp circuit 33. The soft turn-off circuit 32 of FIG. 9 includes an inverter IV31, a resistor element R11 which is coupled in series between a gate IGBT\_GATE of the power semiconductor element Q7 and a ground node, and an NMOS transistor Q11.

[0077]

The mirror clamp circuit 33 includes an inverter IV32, a ninth delay circuit 39, a NAND gate G31, an inverter IV33, a third comparator 40, a NAND gate G32, an inverter IV34, and an NMOS transistor Q12.

[0078]

A /Q output signal of the S/R flip-flop 38 in the overcurrent detection circuit 31 of FIG. 8 is input to the inverter IV31. The /Q output signal becomes low at the time of detecting an overcurrent. Thus, an output of the inverter IV31 becomes high, the NMOS transistor Q11 is turned on, a gate voltage VIGBT\_GATE of the power semiconductor element Q7 is slowly decreased by a time constant which is determined by the resistor element R11 and a capacitance of the NMOS transistor Q11. A reason why the gate voltage VIGBT\_GATE of the power semiconductor element Q7 is slowly decreased in this way is that there is a possibility that the power semiconductor element Q7 may cause latch-up, if the gate voltage VIGBT\_GATE of the power semiconductor element Q7 is rapidly decreased.

[0079]

Meanwhile, a gate voltage VGN2 (output signal of the inverter IV16) of the second PMOS transistor Q5 is input to the inverter IV32 in the mirror clamp circuit 33. The ninth delay circuit 39 delays an output signal of the inverter IV32 by the eighth time. The NAND gate G31 outputs a logical product inversion signal of an output signal of the inverter IV32 and an output signal of the ninth delay circuit 39. The inverter IV33 inverts an output signal of the NAND gate G31 and outputs the inverted signal.

[0080]

The third comparator 40 outputs 5 V if the gate voltage VIGBT\_GATE of the power semiconductor element Q7 is lower than 2.5 V, and outputs 0 V if the gate voltage is equal to or higher than 2.5 V. The inverter IV34 inverts an output signal of the NAND gate G32, outputs the inverted signal, and inputs the output signal to a gate of the NMOS transistor Q12. A voltage value of 2.5 V which is compared by the third comparator 40 is an example, and may be an arbitrary voltage in a range between 2 V and 3.5 V.

[0081]

A drain of the NMOS transistor Q12 is coupled to a gate IGBT\_GATE of the power semiconductor element Q7, and a source thereof is coupled to a ground node. The NMOS transistor Q12 is turned on if the gate voltage VIGBT\_GATE of the power semiconductor element Q7 is lower than 2.5 V, and sharply lowers the gate voltage VIGBT\_GATE of the power semiconductor element Q7 to a ground potential.

[0082]

In this way, at the time of overcurrent, the soft turn-off circuit 32 first operates, the gate voltage VIGBT\_GATE of the power semiconductor element Q7 slowly decreases, and if the gate voltage is lower than 2.5 V, the mirror clamp circuit 33 operates, and an operation in which the gate voltage VIGBT\_GATE of the power semiconductor element Q7 is sharply decreased is performed.

[0083]

A reason why such an operation is performed is that, if the gate voltage VIGBT\_GATE of the power semiconductor element Q7 is lowered to 2.5 V, there is no possibility that latch-up may occur, and thus a gate voltage is rapidly decreased and time required for turning off is reduced.

[0084]

FIG. 10 and FIG. 11 are circuit diagrams illustrating examples of internal configurations of the restart circuit 34 and the first to third timing control units 3 to 5 according to a fourth embodiment. The restart circuit 34 illustrated in FIG. 10 includes an OR gate G33, an S/R flip-flop 41, and an inverter IV35.

[0085]

The OR gate G33 outputs a logical sum signal of the power-on-reset signal POR and a restart signal RESTART. The S/R flip-flop 41 is set at the time of an overcurrent state, and in addition, is reset when an output signal of the OR gate G33 is in a high level.

[0086]

The first timing control unit 3 illustrated in FIG. 10 includes an AND gate G40 with three inputs which is replaced with the AND gate G11 with two inputs in the first timing control unit 3 in FIG. 4. The AND gate G40 outputs a logical product signal of a signal having the same logic as the input signal PWM, a signal which is obtained by delaying the input signal PWM by the first time using the first delay circuit 6, and an output signal of the S/R flip-flop 41 in the restart circuit 34 of FIG. 10.

[0087]

The second timing control unit 4 illustrated in FIG. 10 includes an inverter IV41, a NAND gate G41, and an OR gate G42, in addition to the circuit configuration of the second timing control unit 4 of FIG. 4. An output of the inverter IV41 becomes low at the time of an overcurrent. The NAND gate G41 outputs a logical product inversion signal of an output of the AND gate G41 and an output of the inverter IV41. An output of the NAND gate G41 is input to the NAND gate G1 and the inverter IV6. The OR gate G42 outputs a logical sum signal of the gate signal CL\_GATE of the NMOS transistor in the mirror clamp circuit 33 illustrated in FIG. 9, and an output signal of the level-down circuit 12. An output signal of the OR gate G42 is input to the second delay circuit 7.

[0088]

FIG. 10 and FIG. 11 are circuit diagrams illustrating an internal configuration of the third timing control unit 5. The third timing control units 5 in FIG. 10 and FIG. 11 includes OR gates G43 and G45, inverters IV42 and IV43, an AND gate G44, and the NAND gate G46 with three inputs instead of the NAND gate G14 with two inputs in FIG. 4, which are added to the circuit configuration of the third timing control unit 5 in FIG. 4.

[0089]

The OR gate G45 outputs a logical sum signal of an output signal of the inverter IV14 and a signal 2dan\_err\_H in the overcurrent detection circuit 31 in FIG. 8. The NAND gate G46 outputs a logical product inversion signal of an output signal of the fourth delay circuit 21, an output signal of the inverter IV18, and a signal 2dan\_err\_L in the overcurrent detection circuit 31 in FIG. 8.

[0090]

FIG. 12 is a signal waveform diagram of a gate drive circuit according to the fourth embodiment. A collector current Ix of the power semiconductor element Q7 gradually increases between times t11 and t12. The collector current Ix temporarily becomes zero in time t12, but the collector current Ix gradually increases between times t13 and t14, by using the collector current Ix in time t12 as a starting point. In the same manner, also after time t15, the collector current Ix gradually increases by using the collector current Ix in time t14 as a starting point. However, at the time of t16, the overcurrent detection circuit 31 detects that it is in an overcurrent state, and a Q output signal VSC\_H of the S/R flip-flop 38 in the overcurrent detection circuit 31 becomes high. As a result, a gate voltage of the high-side PMOS transistor Q1 which is in an ON state becomes high, and thereby the high-side PMOS transistor Q1 is turned off. When an overcurrent is detected, the low-side NMOS transistor Q4 is in an OFF state, and thus is maintained as an OFF state as it is.

[0091]

In addition, a gate voltage of the NMOS transistor Q11 in the soft turn-off circuit 32 becomes low. Thus, the gate voltage VIGBT\_GATE of the power semiconductor element Q7 gradually decreases by the soft turn-off circuit 32 (times t16 to t17).

[0092]

If the gate voltage VIGBT\_GATE of the power semiconductor element Q7 is lower than 3.5 V, the output signal 2dan\_err\_H in the overcurrent detection circuit 31 becomes low, and the output signal 2dan\_err\_L becomes high. As a result, a gate voltage of the first PMOS transistor Q2 becomes low, and the first PMOS transistor Q2 is turned on. Thus, the low-side NMOS transistor Q4 is turned on, and force to decrease the gate voltage VIGBT\_GATE of the power semiconductor element Q7 is increased. Thereafter, if the gate voltage VIGBT\_GATE of the power semiconductor element Q7 becomes lower than 2.5 V, the NMOS transistor Q12 in the mirror clamp circuit 33 is turned on, and the gate voltage VIGBT\_GATE of the power semiconductor element Q7 sharply decreases to a ground potential (time t18).

[0093]

Thereafter, even if the input signal PWM becomes high again in time t20, the S/R flip-flop 38 in the overcurrent detection circuit 31 in FIG. 8, and the S/R flip-flop 41 in the restart circuit 34 in FIG. 14 are maintained in a set state. Thus, an ON drive of the power semiconductor element Q7 is not performed.

[0094]

Thereafter, if the restart signal becomes high in time t22, the S/R flip-flop 41 in the restart circuit 34 in FIG. 10 enters a reset state, a Q output of the S/R flip-flop 41 becomes low, and /Q output thereof becomes high. Thus, an output of the inverter IV35 becomes low. At this time, if the input signal PWM is low, an output of the OR circuit G43 becomes low, an output of the inverter IV42 on the subsequent side thereof becomes high. Thus, an output of the OR gate G22 in the overcurrent detection circuit 31 in FIG. 8 becomes high, the S/R flip-flop 38 enters a reset state, an overcurrent detection signal SC\_H becomes low, and an overcurrent state is reset.

[0095]

As a result, thereafter, in a time point (time t23) in which the input signal PWM is high, an operation of driving the power semiconductor element Q7 to be turned on is performed. However, if an overcurrent is detected in time t24 immediately after the time t23, the gate voltage VIGBT\_GATE of the power semiconductor element Q7 is gradually decreased (times t24 to t25) by the soft turn-off circuit 32, in the same manner as in times t16 to t19. Thereafter, the gate voltage is sharply decreased by the mirror clamp circuit 33 (times t25 to t26).

[0096]

In this way, the gate drive circuit according to the fourth embodiment gradually decreases the gate voltage VIGBT\_GATE of the power semiconductor element Q7, if the collector current Ix of the power semiconductor element Q7 enters an overcurrent state, and sharply decreases the gate voltage, if the gate voltage is decreased to a voltage level in which latch-up does not occur. As a result, it is possible to prevent the latch-up and to reduce an OFF time. In addition, if an overcurrent state is detected, ON-driving of the power semiconductor element Q7 is temporarily stopped, and thereafter, if the restart signal becomes high, the ON-driving of the power semiconductor element Q7 is started, and thereby the power semiconductor element Q7 can be stably driven.

[0097]

While certain embodiments have been described, these embodiments have been presented by way of example only, and are not intended to limit the scope of the inventions. Indeed, the novel embodiments described herein may be embodied in a variety of other forms; furthermore, various omissions, substitutions and changes in the form of the embodiments described herein may be made without departing from the spirit of the inventions. The accompanying claims and their equivalents are intended to cover such forms or modifications as would fall within the scope and spirit of the inventions.

WHAT IS CLAIMED IS:

1. A gate drive circuit comprising:

a first PMOS transistor that is coupled between a first reference voltage node and a first output node;

a first NMOS transistor that is coupled between the first output node and a second reference voltage node whose voltage level is lower than that of the first reference voltage node;

a second PMOS transistor that is coupled between the first reference voltage node and a second output node;

a second NMOS transistor that is coupled between the second output node and the second reference voltage node; and

a gate control circuit that generates each gate signal of the first PMOS transistor, the first NMOS transistor, the second PMOS transistor, and the second NMOS transistor based on an input signal,

wherein the gate control circuit includes,

a first timing control unit that, before a potential of the first output node is decreased from a high potential to a low potential, decreases a potential of the second output node from a high potential to a low potential, and before a potential of the second output node is increased from a low potential to a high potential, increases a potential of the first output node from a low potential to a high potential;

a second timing control unit that, before one of the first PMOS transistor and the first NMOS transistor is changed from OFF to ON, changes the other of those from ON to OFF, and before the other is changed from OFF to ON, changes the one from ON to OFF; and

a third timing control unit that, before one of the second PMOS transistor and the second NMOS transistor is changed from OFF to ON, changes the other of those from ON to OFF, and after the one is changed from ON to OFF, changes the other from OFF to ON.

2. The circuit according to Claim 1,

wherein the first timing control unit includes a first delay circuit that delays the input signal by a first time, and

wherein the second timing control unit and the third timing control unit shift timing in which potentials of the first output node and the second output node are changed, using the first time.

3. The circuit according to Claim 1 or 2,

wherein the second timing control unit includes,

a second delay circuit that raises a gate signal of the first NMOS transistor by delaying by a second time from rising timing of a gate signal of the first PMOS transistor; and

a third delay circuit that lowers a gate signal of the first PMOS transistor by delaying by a third time from falling timing of a gate signal of the first NMOS transistor, and

wherein the third timing control unit includes,

a fourth delay circuit that raises a gate signal of the second NMOS transistor by delaying by a fourth time from rising timing of a gate signal of the second PMOS transistor; and

a fifth delay circuit that lowers a gate signal of the second PMOS transistor by delaying by a fifth time from falling timing of a gate signal of the second NMOS transistor.

4. The circuit according to any one of Claims 1 to 3, further comprising:

an overcurrent detection circuit that detects whether or not an output current of a fifth transistor which is controlled by a third transistor that is controlled by a voltage of the first output node, and by a fourth transistor that is controlled by a voltage of the second output node, is in an overcurrent state,

wherein if the overcurrent state is detected, the gate control circuit sets the first output node to a high potential and sets the second output node to a low potential.

5. The circuit according to Claim 4, further comprising:

an impedance element and a sixth transistor which are coupled in series between a gate of the fifth transistor and the second reference voltage node,

wherein, if the overcurrent state is detected, the gate control circuit turns on the sixth transistor.

6. The circuit according to Claim 4 or 5, further comprising:

a first voltage detection circuit that detects whether or not a gate voltage of the fifth transistor is equal to or lower than a first voltage,

wherein, in a state in which the overcurrent state is detected, if the first voltage detection circuit detects that the gate voltage of the fifth transistor is equal to or lower than the first voltage, the gate control circuit changes a potential of the second output node from a low potential to a high potential.

7. The circuit according to Claim 6, further comprising:

a second voltage detection circuit that detects whether or not a gate voltage of the fifth transistor is a second voltage which is lower than the first voltage,

wherein the gate control circuit includes a seventh transistor that, in a state in which the overcurrent state is detected, if the second voltage detection circuit detects that the gate voltage of the fifth transistor is equal to or lower than the second voltage, lowers a gate voltage of the fifth transistor to a low voltage.

8. The circuit according to any one of Claims 4 to 7,

wherein the gate control circuit includes a restart circuit that, in a state of a temporary overcurrent state, maintains a high potential of the first output node and a low potential of the second output node, until a first signal or a second signal becomes a predetermined logic, and if the first signal or the second signal becomes the predetermined logic, changes potentials of the first output node and the second output node, according to logic of the input signal.

9. A gate drive circuit comprising:

a first PMOS transistor that is coupled between a first reference voltage node and a first output node;

a first NMOS transistor that is coupled between the first output node and a second reference voltage node whose voltage level is lower than that of the first reference voltage node;

a second PMOS transistor that is coupled between the first reference voltage node and a second output node; and

a second NMOS transistor that is coupled between the second output node and the second reference voltage node,

wherein a potential of the first output node does a first change from a high potential to a low potential, a potential of the second output node is changed from a high potential to a low potential before the first change, a potential of the second output node does a second change from a low potential to a high potential, and a potential of the first output node is changed from a low potential to a high potential before the second change,

wherein before one of the first PMOS transistor and the first NMOS transistor is changed from OFF to ON, the other of those is changed from ON to OFF, and before the other is changed from OFF to ON, the one is changed from ON to OFF, and

wherein before one of the second PMOS transistor and the second NMOS transistor is changed from OFF to ON, the other is changed from ON to OFF, and after the one is changed from ON to OFF, the other is changed from OFF to ON.

ABSTRACT

According to one embodiment, a gate control circuit in a gate drive circuit includes a first timing control unit that, before a potential of the first output node is decreased from a high potential to a low potential, decreases a potential of the second output node from a high potential to a low potential, and before a potential of the second output node is increased from a low potential to a high potential, increases a potential of the first output node from a low potential to a high potential; a second timing control unit that, before one of the first PMOS transistor and the first NMOS transistor is changed from OFF to ON, changes the other of those from ON to OFF, and before the other is changed from OFF to ON, changes the one from ON to OFF; and a third timing control unit that before one of the second PMOS transistor and the second NMOS transistor is changed from OFF to ON, changes the other of those from ON to OFF, and after the one is changed from ON to OFF, changes the other from OFF to ON.

Drawings

FIG. 1

3: FIRST TIMING CONTROL UNIT

4: SECOND TIMING CONTROL UNIT

5: THIRD TIMING CONTROL UNIT

2: GATE CONTROL CIRCUIT

1: GATE DRIVE CIRCUIT

FIG. 7

3: FIRST TIMING CONTROL UNIT

4: SECOND TIMING CONTROL UNIT

34: RESTART CIRCUIT

5: THIRD TIMING CONTROL UNIT

2: GATE CONTROL CIRCUIT

33: MIRROR CLAMP CIRCUIT

32: SOFT TURN-OFF CIRCUIT

31: OVERCURRENT DETECTION CIRCUIT